EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	589	synchroniz$5 near3 clock$1 near5 semiconductor	USPAT	OR	OFF	2006/12/13 11:17
S2	3	synchroniz$5 near3 clock$1 near5 semiconductor same master same slave	USPAT	OR	OFF	2006/12/13 11:18
S3	1	synchroniz$5 near3 clock$1 near5 semiconductor same master same slave	US-PGPUB	OR	OFF	2006/12/13 11:20
S4	1	synchroniz$5 near3 clock$1 near5 semiconductor same master same slave	EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 11:21
S5	0	lowest adj rate with master	USPAT	OR	OFF	2006/12/13 11:22
S6	639	master adj device with slave adj devices	USPAT	OR	OFF	2006/12/13 11:24
S7	85	master adj device with slave adj devices with clock	USPAT	OR	OFF	2006/12/13 11:24
S8	0	master adj device with slave adj devices with clock same phase$1align$3	USPAT	OR	OFF	2006/12/13 11:26
S9	0	master adj device with slave adj devices with clock adj sources	USPAT	OR	OFF	2006/12/13 11:26
S10	13	master adj device with slave adj devices with clock with (lowest least common)	USPAT	OR	OFF	2006/12/13 11:27
S11	12	master adj device with slave adj devices with clock with (lowest least common)	US-PGPUB	OR	OFF	2006/12/13 11:33
S12	1	master adj device with slave adj devices with clock with (lowest least common)	EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 11:34
S13	1	master with common adj denominator with clock	USPAT	OR	OFF	2006/12/13 11:44
S14	2	master with common adj denominator with clock	US-PGPUB; EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 11:45
S15	4	phase$1align$3 with clock with master	USPAT	OR	OFF	2006/12/13 11:47
S16	2	phase$1align$3 with clock with master	US-PGPUB	OR	OFF	2006/12/13 11:48
S17	0	phase$1align$3 with clock with master	EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 11:48
S18	2	phase$1align$3 with clock with slave	USPAT	OR	OFF	2006/12/13 11:50
S19	2	phase$1align$3 with clock with slave	US-PGPUB	OR	OFF	2006/12/13 11:51
S20	0	phase$1align$3 with clock with slave	EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 11:51

EAST Search History

S21	39	(lowe$2 slow$3) adj clock near5 master	USPAT	OR	OFF	2006/12/13 13:05
S22	7	(lowe$2 slow$3) adj clock near5 master same slave	USPAT	OR	OFF	2006/12/13 13:03
S23	5	(lowe$2 slow$3) adj clock near5 master same slave	US-PGPUB	OR	OFF	2006/12/13 13:04
S24	0	(lowe$2 slow$3) adj clock near5 master same slave	EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 13:05
S25	11	(lowe$2 slow$3) adj clock near5 master	US-PGPUB	OR	OFF	2006/12/13 13:10
S26	1	(lowe$2 slow$3) adj clock near5 master	EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 13:11
S27	21	master$1slave adj configuration near5 synchroniz$5	USPAT	OR	OFF	2006/12/13 13:21
S28	8	master$1slave adj configuration near5 synchroniz$5	US-PGPUB	OR	OFF	2006/12/13 13:25
S29	0	master$1slave adj configuration near5 synchroniz$5	EPO; JPO; IBM_TDB	OR	OFF	2006/12/13 13:25
S30	0	lee.in. with de-wei	USPAT	OR	OFF	2006/12/13 13:31
S31	30	lee.in. and benq.as.	USPAT	OR	OFF	2006/12/13 13:31
S32	1	yang.in. with wu-han	USPAT	OR	OFF	2006/12/13 13:33
S33	21	yang.in. and benq.as.	USPAT	OR	OFF	2006/12/13 13:33
S34	847	713/500.ccls.	USPAT	OR	OFF	2006/12/13 13:34
S35	0	713/500.ccls. and synchroniz$5 near3 clock$1 near5 semiconductor same master same slave	USPAT	OR	OFF	2006/12/13 13:40
S36	0	713/500.ccls. and master adj device with slave adj devices with clock with (lowest least common)	USPAT	OR	OFF	2006/12/13 13:41
S37	0	713/500.ccls. and master with common adj denominator with clock	USPAT	OR	OFF	2006/12/13 13:42
S38	0	713/500.ccls. and (lowe$2 slow$3) adj clock near5 master same slave	USPAT	OR	OFF	2006/12/13 13:42
S39	0	713/500.ccls. and master$1slave adj configuration near5 synchroniz$5	USPAT	OR	OFF	2006/12/13 13:43
S40	0	713/500.ccls. and phase$1align$3 with clock with master	USPAT	OR	OFF	2006/12/13 13:43
S41	1044	713/400.ccls.	USPAT	OR	OFF	2006/12/13 13:50
S42	2	713/400.ccls. and master adj device with slave adj devices with clock with (lowest least common)	USPAT	OR	OFF	2006/12/13 14:00
S43	0	713/400.ccls. and phase$1align$3 with clock with master	USPAT	OR	OFF	2006/12/13 14:01

EAST Search History

S44	0	713/400.ccls. and master$1slave adj configuration near5 synchroniz$5	USPAT	OR	OFF	2006/12/13 14:03
S45	0	713/400.ccls. and (lowe$2 slow$3) adj clock near5 master same slave	USPAT	OR	OFF	2006/12/13 14:03
S46	0	713/400.ccls. and master with common adj denominator with clock	USPAT	OR	OFF	2006/12/13 14:04
S47	0	713/400.ccls. and synchroniz$5 near3 clock$1 near5 semiconductor same master same slave	USPAT	OR	OFF	2006/12/13 14:04
S48	682	375/356.ccls.	USPAT	OR	OFF	2006/12/13 14:05
S49	0	375/356.ccls. and master adj device with slave adj devices with clock with (lowest least common)	USPAT	OR	OFF	2006/12/13 14:10
S50	0	375/356.ccls. and phase$1align$3 with clock with master	USPAT	OR	OFF	2006/12/13 14:10
S51	1	375/356.ccls. and master$1slave adj configuration near5 synchroniz$5	USPAT	OR	OFF	2006/12/13 14:11
S52	0	375/356.ccls. and (lowe$2 slow$3) adj clock near5 master same slave	USPAT	OR	OFF	2006/12/13 14:11
S53	0	375/356.ccls. and master with common adj denominator with clock	USPAT	OR	OFF	2006/12/13 14:12
S54	0	375/356.ccls. and synchroniz$5 near3 clock$1 near5 semiconductor same master same slave	USPAT	OR	OFF	2006/12/13 14:12